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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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027260-468	09/879,197
APPLICANT: Michio KOMODA et al.	
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U.S. PATENT DOCUMENTS

Examiner Initials	U.S. Patent Document Number	U.S. Patent Document Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication (MM-DD-YYYY)

FOREIGN PATENT DOCUMENTS

Examiner Initials	Foreign Patent Document Number	Foreign Patent Document Kind Code (if known)	Country	Date of Publication (MM-DD-YYYY)	Translation Yes	Translation no
[illegible]	JP-A 9-211087		JAPAN	08-15-1997	Abst	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
[illegible]	"Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation", Proc. IEEE International Conference on Computer Aided Design, 1989, Peter R. O'BRIEN et al., IEEE
[illegible]	"A Gate-Delay Model for High-Speed CMOS Circuits", Proc. 31st ACM/IEEE Design Automation Conference, 1994, Florentin DARTU et al., The University of Texas at Austin, Austin, Texas 78712
[illegible]	U.S. Application No. 09/878,352, Michio KOMODA et al., " Method of Producing Load for Delay Time Calculation and Recording Medium", June 12, 2001

Examiner Signature	[illegible]	Date Considered	5/1/04

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(05/01)